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Cross-sectional study of engineering student performance across different types of first-year digital logic design laboratories

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Cross-sectional study of engineering student performance across different types of first-year digital logic design laboratories

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Abstract - **As a follow-on to our previous effort of designing the lecture and lab courses that would apply to a predominantly Aerospace and Mechanical Engineering (AE/ME) undergraduate cohort, this cross-sectional study aims to examine the effect of different types of laboratories on material retention and success in upper level courses. We tracked the performance of each of the 159 students who took part in this study throughout the semester, culminating in a laboratory final that involves applying concepts learned in a practical setting under strict timing constraints.**

Data show that students attained a more even level of understanding across multiple topics, could apply digital logic design concepts to real-world design problems, and effortlessly used industry standard equipment and tools when the laboratories were blended between "manual wiring" / "cookbook" and "virtual wiring" / "system design" types of experiments.

This study provides results that may help other first year engineering departments in designing new courses or laboratory curricula.

Index Terms - Industry-standard tools, electrical engineering for non-majors, first-year engineering, material retention.

INTRODUCTION

Improving on our earlier work of designing a new digital circuit design laboratory sequence for first-year engineering students and non-majors [1], we deployed three types of digital circuits laboratory sequences across four laboratory sections at Embry-Riddle Aeronautical University—a small, teaching university in the Southwest, focused on the aerospace and mechanical engineering (AE/ME) disciplines. The three variations of laboratories included older "cookbook-style" labs based on manual wiring (control group), newer-style laboratories with a heavy emphasis on VHDL and virtual wiring techniques using industry standard tools, and a hybrid section that balanced concepts from the two laboratories. We compared student performance on seven questions that tested various facets of the laboratory (including design) across all three laboratory types. Both the test and control groups had a similar breakdown by student academic major.

I. Background and Motivation

In prior semesters, the laboratory comprised of material largely applicable to electrical and computer engineering (EE/CE) students, had little integration with industry standard tools and equipment, and used a "cookbook lab" approach, with a limited perspective on system design. It was found [1] that most students could not connect the concepts from the laboratory to any practical applications and had low perceptions of applicability of the material to their major, based on an exit survey administered at the end of the semester.

Addressing these concerns, we designed a new laboratory sequence that was piloted across two sections of the class in the Spring of 2016 alongside two control sections (using the older "cookbook" approach). The original intention was to increase the amount of hands-on learning to raise the level of student interest and motivation in the lab course, per the findings in [2]. The new lab sequence required the use of field-programmable gate array (FPGA) development boards, the VHSIC hardware description language (VHDL), and industry-standard design tools, such as Xilinx Vivado. Prior research has shown that introducing concurrent processing and FPGA devices into the ME curriculum had positive impact on the perceptions of value of the learned material among students taking the course [3]. AE/ME students could also use this knowledge in follow-on or capstone design [4] courses.

The students learned how to integrate sensors, motors, and encoders with state-of-the-art digital hardware. Using electronic design automation (EDA) tools lowered the level of abstraction through the use of "virtual wiring" and introduced students to in-depth troubleshooting techniques. Exit surveys showed a significant increase in positive student perceptions of the lab and its applicability to their major/upper-level courses. Research has shown that computer-based tools stimulate students toward exploring topics on their own and completing more advanced projects, that would not be otherwise possible in a laboratory setting [5,6]. From a department perspective, enrollments in the laboratory can also increase without detrimental effects to student learning [7].

Despite positive student perceptions, the new laboratory sequence did little to introduce the students to discrete elec-

tronic components (*i.e.*, resistors, integrated circuits, breadboards)—a skill required in some upper-level courses for rapid prototyping and testing of student designs.

In Spring of 2017, we developed an additional laboratory sequence, dubbed "hybrid", which combined the best aspects from both old-style labs that used discrete components almost exclusively and the Spring 2016 sequence that used primarily EDA tools. A laboratory final examination (LFE) was developed to test individual student performance against the learning outcomes (LOs) listed in the "Master Course Outline" (MCO).

II. Course Content

Embry-Riddle has two residential campuses, both of which must agree on an MCO that provides a blueprint of all required concepts within a course and learning outcomes that students should achieve by the course's conclusion. To maintain consistency of the material taught between multiple sections, each instructor should cover at least 75% of the MCO topics and outcomes.

The LOs from the CEC222 MCO [8] are listed below. All of the LOs relate, with various degrees of intersection, to ABET Criterion 3 [9], student learning outcomes A-K (with particular emphasis on B-G and K, which get introduced in this course). At the conclusion of the laboratory sequence, students should be able to:

1. Design, construct, troubleshoot digital circuits (*BCE*).
2. Interface digital circuitry with external devices (*BC*).
3. Use numbering systems and number conversions (*E*).
4. Apply Boolean algebra to simplify expressions (*BCEK*).
5. Utilize logic gates, explain their function (*EG*).
6. Construct truth tables (*E*).
7. Use a logic simulator (*K*).
8. Use standard lab equipment (*e.g.*, oscilloscope), (*BK*).
9. Interpret manufacturer device data sheets (*G*).
10. Design and build combinational logic circuits (*B*).
11. Design and build sequential logic circuits (*B*).
12. Analyze electronic circuits (*BG*).
13. Use and explain operation of integrated circuits (*GK*).
14. Design a circuit using flip-flops, decoders, multiplexers, adders, comparators, shift registers (*BC*).
15. Explain the operation of the above devices (*G*).
16. Analyze combinational and sequential logic circuits (*E*).
17. Explain operation of programmable logic devices (*GK*).
18. Analyze timing of logic circuits and be able to derive a logic circuit timing diagram (*B*).

III. Overview of Similar Pedagogies

In the new (EDA) laboratory sequence from Spring 2016 and the revamped "hybrid" implementation, we used scaffolding to advance the students from simple to more advanced concepts. Both the EDA and hybrid implementations featured project-based learning (PBL). Similar projects that improved student motivation can be found at the University of South Australia, where courses taken during the first year are similar across engineering disciplines [10]. Since the laboratory course at Embry-Riddle used two teaching assistants and students were paired up with a partner, the implementation was similar to [11], where a *floating facilitator* assisted with the PBL approach.

IMPLEMENTATION OVERVIEW

To test the effectiveness of the three approaches (control, EDA, and hybrid), we designed a laboratory final examination. The laboratory final examination covered most of the LOs from the MCO. By comparing all three sections, advantages/drawbacks of each approach could be clearly seen.

The content of each question is provided in Table I. A general description of the problem is given for context.

TABLE I
CONCEPTS/LOS TESTED ON FINAL LABORATORY EXAMINATION

No.	MCO LO	Pts.	Exam Concepts Tested
1-A	*8*	10	Identify resistors based on their color code, build a resistive circuit, connect the input to a 5 V supply and measure the voltage at the output. Resistor color code is given in the reference booklet.
1-B	*8, (2)*	10	Measure a mystery waveform using an oscilloscope, trigger the oscilloscope on the leading edge of the waveform, provide the period and peak-to-peak voltage of the waveform.
2	*11, 18, (12, 14–16)*	10	Analyze a sequential circuit and provide its timing diagram.
3	*1, 9, 10, (2, 13)*	20	Build a combinational logic circuit using discrete components, connect to power and outputs. Data sheets for common components provided in reference booklet.
4	*5, 7, (17*)*	15	Implement a logic circuit in VHDL and simulate all possibilities with the logic simulator.
5	*3, 4, 12, (13, 16)*	20	Read out the truth table from an existing circuit, extract minterm/maxterm expression, and simplify using any method.
6	*4, 5, 6, 10*	15	Minimize the expression using Karnaugh maps, implement the circuit using the fewest types of logic gates (on paper).

Exam questions were staggered in a way that allowed the teaching assistants and instructors to check the student work as they were working on the next problem (the first few problems required a demo of the circuit or the triggering of the oscilloscope). Since a detailed rubric was created ahead of time for each question, it was possible to grade responses "on the fly" while referencing the student set-ups. As a test of the rubric, ungraded questions were provided to undergraduate teaching assistants (TAs) for grading. Both TAs and the instructor graded the questions identically, proving the robustness of the created rubric. Each question was individually timed and no students were allowed to exit the examination room until the end of the period.

According to the rubric, a raw score, in addition to one of four performance indicators, was assigned for each problem. Performance indicators used are similar to what ABET utilizes for their rubrics: Unsatisfactory (**U**), Developing (**D**), Acceptable (**A**), and Exemplary (**E**). To visualize the data, these performance indicators were recoded into 1-4, respectively.

TABLE II
PROBLEM 1 RUBRIC

Part A (10 pts): Identify resistors based on their color code, build a resistive circuit, connect the input to a 5 V supply and measure the voltage at the output. Resistor color code is given in the reference booklet.

Ind.	Pts.	Description
	1	Connects any voltage / any resistors but shorts them out
U	1	Cannot determine the correct resistors to use
	3	Can determine the correct resistors to use but they may be reversed (so incorrect circuit implemented)
D	4	Can connect 5V and resistors to the board without shorting in the same column
	5	Can determine the correct resistors to use and put them correctly on the board
A	7	Can connect 5V and resistors to the board without shorting and **connect the voltage measuring device**
E	10	Measures the correct voltage using the correct resistors and 5V

Part B (10 pts): Measure a mystery waveform using an oscilloscope, trigger the oscilloscope on the leading edge of the waveform, provide the period and peak-to-peak voltage of the waveform.

Ind.	Pts.	Description
	1	Did not connect the board to the scope
U	1	Did not open o-scope software or opened the software in demo mode
	3	Can open the oscilloscope software
	4	Can connect Basys3 board to O-Scope
D	5	Can open the o-scope software and **show a waveform on the screen**
	6	Uses the **digital logic analyzer** to measure period but **cannot determine voltage**
	7	**Shows full waveform with trigger but both period and voltage incorrect**
A	8	**Shows full waveform with trigger but either period or voltage incorrect** (–1 if stopped)
	8	Shows the full waveform in analog with correct values and **one minor error**: stopped instead of triggered, AC instead of DC biased
E	10	**Shows the full waveform in analog triggered with correct values for period and voltage**

TABLE III
PROBLEM 2 RUBRIC

(10 pts) Analyze a sequential circuit and provide its timing diagram.

Ind.	Pts.	Description
	2	Waveform drawn does not follow input in any way (random)
	3	Waveform does not follow input and follows a clock edge at least once
U	4	Waveform is random and follows rising edge at least once and shows input propagation
	5	Wrong period, rising or falling edge, **follows input at least once**
	6	Waveform has **wrong period** (It is longer or shorter than one clock period) and **follows rising edge at least once**
D	7	Waveform has **correct period** and follows rising edge at least once
	8	Waveform follows rising edge but is of the **wrong period**
	9	Waveform is of correct duration but **follows falling edge**
A	9	Waveform is the correct duration and follows the rising edge but **not on all of the outputs**
E	10	Waveform is of the **correct duration and follows the rising edge trigger on all of the outputs** from the chips

TABLE IV
PROBLEM 3 RUBRIC

(20 pts) Build a combinational logic circuit using discrete components, connect to power and outputs. Data sheets for common components provided in reference booklet.

Ind.	Pts.	Description
	0	Nothing wired
	1	Only clock module connected / Some wires, no ICs
	2	Some number of ICs placed on the board
	3	Some ICs and wires
U	4	Power and ground and some ICs
	5	Random wires connected from Basys3 to circuit with **some number of ICs**
	6	**Correct number of ICs** but obviously incomplete circuit
	7	The correct number **and type** of ICs were used but an obviously incomplete circuit
	8	The correct number and type of ICs were used and it was **connected to the Basys3 board** but the rest was an **obviously incomplete circuit**. (i.e. Missing Power)
D	9	The correct number and type of ICs were used and it was connected to the Basys3 board and the ICs were powered, but the rest was an **obviously incomplete circuit**
	11	The correct number and type of ICs were used and it was connected to the Basys3 board to the **wrong Pmod port or power/ground reversed**
	12	The correct number and type of ICs were used and it was connected to the Basys3 board to the **correct Pmod port**
	14	Some failed tests with Basys3 correctly connected to circuit and **obvious wire or two was missing**
A	16	Some failed tests but **unknown source of the error** (looked fine upon cursory inspection)
	18	Some small number of tests failed because of an observed wiring problem, could be fixed with more time/feedback
E	20	No tests failed upon verification

TABLE V
PROBLEM 4 RUBRIC

(15 pts) Implement a logic circuit in VHDL and simulate all possibilities.

Ind.	Pts.	Description
	0	Nothing provided
	2	Can write VHDL by hand
U	3	Can open a program to write VHDL
	4	Can open new VHDL file and write VHDL
	7	Can write combinational logic in VHDL
	9	Creates nets for combinational logic
D	10	Can open a simulator to simulate their VHDL
	11	Can simulate some/all possibilities of an incorrect circuit
	12	Can simulate some possibilities of the correct circuit
A	13	Can simulate all possibilities, but not in logical order
	15	Simulates all possibilities of the correct circuit
E	16	Simulated using a VHDL test bench (+1)

TABLE VI
PROBLEM 5 RUBRIC

(20 pts) Read out the truth table from an existing circuit, extract minterm/maxterm expression, and simplify using any method.

Ind.	Pts.	Description
	1	Draw T.T., wrong input combinations
	2	TT has 16 combinations, inverted values from B3 board or none at all
U	3	TT correct, wrong minterms, missing simplification
	6	TT correct, minterm correct, missing simplification
D	8	TT correct, min. correct, simpl. obviously incomplete
	12	TT correct, minterm correct, simplification not finished
	13	TT, minterm, Kmap correct size/filled, wrong groups circ.
A	16	Not fully minimized expression / extra groups
	18	No minterm expression
E	20	Perfect solution

TABLE VII
PROBLEM 6 RUBRIC

(15 pts) Minimize the expression using Karnaugh maps, implement the circuit using the fewest types of logic gates (on paper).

Ind.	Pts.	Description
	0	Cannot draw a K-map
U	1	Cannot draw correctly sized K-map
	4	Draws a K-map but cannot place 1's and 0's correctly
	5	Draws a K-map and fills in 1's and 0's correctly
	6	Circles groups inside the K-map
	6	2 gate types, incomplete K-map
D	7	Draws a circuit based on the incorrect groups
	8	Draws a circuit with only a single gate type but based upon incorrect K-map
	9	Draws any circuit based on un-minimized groupings
	9	Circles the correct number of groups inside the K-map
	10	Draws any circuit based upon correct K-map groupings
A	11	Draws a circuit with up to 3 gate types, no inverters
	14	Draws a circuit with 2 different gate types and no inverter
E	15	Draws a circuit with only one gate type used

RESULTS

The impact of the hybrid section was evaluated against the control group (older "cookbook"-style laboratories) and the revamped (EDA-based) laboratory experiments from Spring 2016. Plots in Fig. 1 show the mean of indicators and the mean of scores for each of the 6 questions, with parts A and B of question 1 being analyzed separately. The score breakdown is more granular and is therefore a more accurate representation of student abilities. The indicators were recoded as: Exemplary (E) 4, Acceptable (A) 3, Developing (D) 2, and Unsatisfactory (U) 1.

This study included 159 students and the laboratory final examination was given a weight of 30% of the final laboratory course grade. The students completed the final examination individually.

As mentioned, the CEC222 laboratory at Embry-Riddle serves as a "service" course to the largest department on campus: Aerospace and Mechanical Engineering. The academic majors in the class were divided into: AE/ME, EE/CE/Software Engineering (SE), Unmanned Aerospace Systems (UAS), Global Security and Intelligence Studies (GSIS), Cyber Intelligence and Security (CIS), Meteorology (M), Aeronautics (A), Aeronautical Science (AS), and Business (B). Overall, the breakdown of students in each section of the laboratory was similar and can be seen in Table II.

One drawback of this study was that sufficient equipment and exam testing times were not available to us to test all of the students at once. Instead, the students were tested during 8 separate examination periods. Many of the students from the earlier sections spoke with their peers regarding the content and the specifics of each exam question.

In an informal survey of the students in the last two exam sessions (a tally sheet with two columns that was passed around after the exam was taken), both of which included students from the control group, 22 of the 44 students in the sections admitted to having discussed specifics of the question content and seven students admitted to having discussed vague references to the topics on the exam.

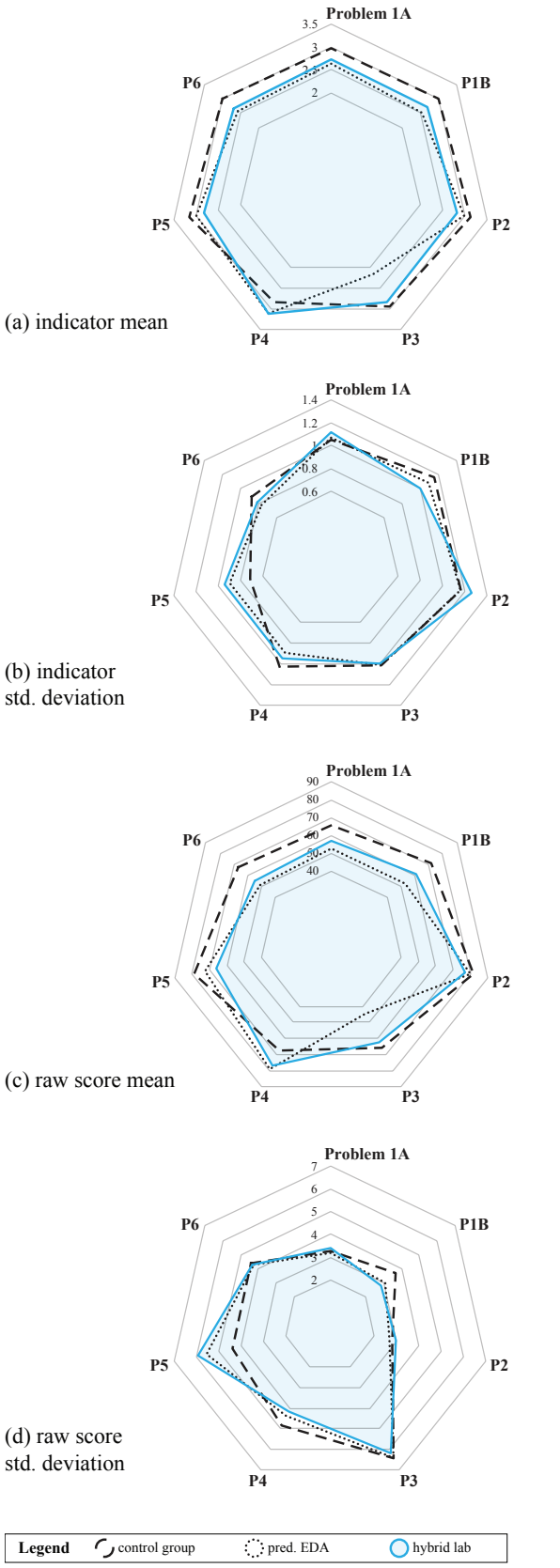


FIGURE 1
RESULTS ACROSS ALL THREE LABORATORY TYPES, BY QUESTION NUMBER.

TABLE VIII
ENROLLED STUDENTS, BY ACADEMIC MAJOR AND GRADE LEVEL

Maj.	Lvl.	Hybrid		Control		EDA	
A						1	1.2%
AE		30	68.2%	28	71.8%	53	61.6%
AS						1	1.2%
B		1	2.3%				
CIS		1	2.3%			1	1.2%
CE				1	2.6%	7	8.1%
EE		2	4.5%	1	2.6%	6	7.0%
GSIS				2	5.1%		
ME		8	18.2%	6	15.4%	13	15.1%
M		1	2.3%				
SE						4	4.7%
UAS		1	2.3%	1	2.6%		
	FR	19	43.2%	16	41.0%	34	39.5%
	SO	18	40.9%	17	43.6%	37	43.0%
	JR	5	11.4%	5	12.8%	12	14.0%
	SR	2	4.5%	1	2.6%	3	3.5%
Total		44		39		86	

* Percentage total may not add to 100% due to rounding error(s).

It would be beneficial to have all three types of sections tested during the same exam period. Despite having multiple exam periods, this would equalize the playing field and provide more accurate results. This exam administration flaw can be seen in high standard deviations for the later sections. Due to this failure, cumulative results across all examination sections cannot be considered at face value.

To remove the "cheating" bias, results from only the first three sections of the final were analyzed; the results are given in Fig. 2. All three sections were administered on the same day, minimizing the crosstalk between class members, and included all of the laboratory variants: control, hybrid, and predominantly EDA-based (in that order, back to back). Since each question was timed individually, no students could leave until the end of the examination period, effectively eliminating information sharing between at least the first two sections of the examination.

Overall, the hybrid section had higher raw scores and lower standard deviations across all of the examination questions. As expected, students from the EDA-based laboratory section scored lower than their peers on Problem 3 (building a combinational logic circuit on the breadboard using discrete components). Some of the common mistakes made are highlighted in Fig. 3.

Another drawback of the designed testing tool is that more advanced EDA tool techniques were not tested (only basic tool familiarity). Despite the students scoring lower on some of the questions, the depth and breadth of knowledge that the students from the hybrid section have is much higher than what could have been evaluated.

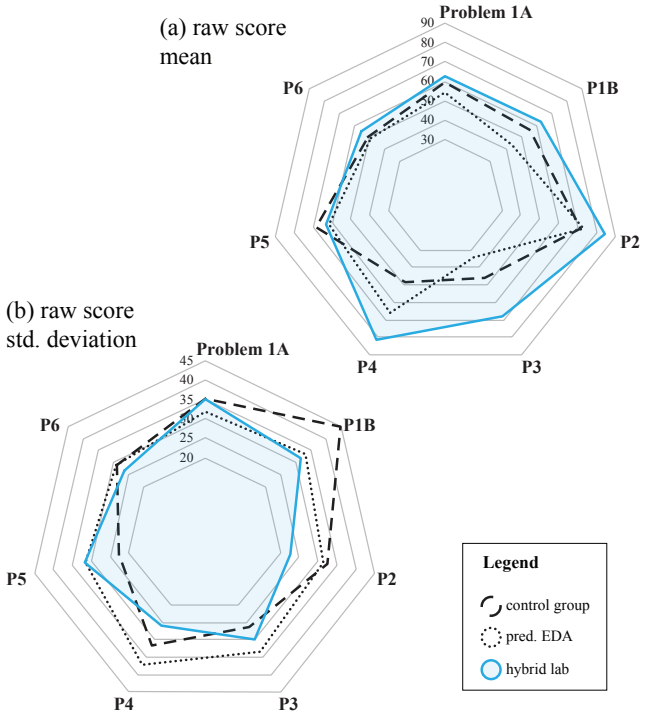
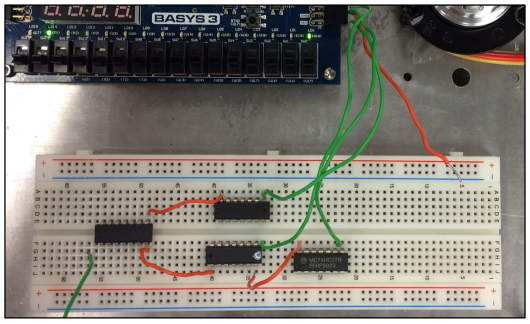
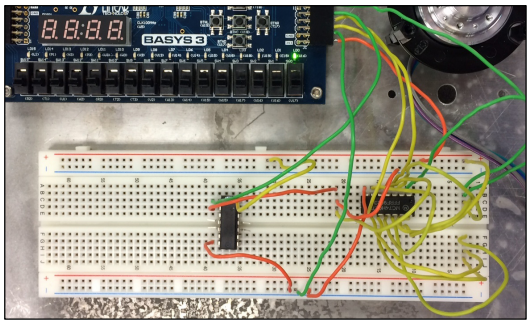


FIGURE 2
RESULTS ACROSS ALL THREE LABORATORY TYPES, BY QUESTION NUMBER; WITH "CROSSTALK BIAS" ELIMINATED.



(a) Student board with incorrect number of ICs. The three ICs on the right side of the breadboard are shorted together. No power/ground connections.



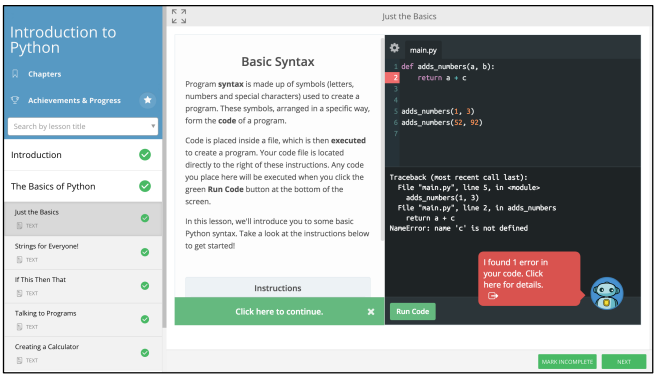
(b) Student board with correct number of ICs, positioned incorrectly on breadboard (IC on left is positioned over the separating channel, pins bent).

FIGURE 3
A SAMPLING OF "UNSATISFACTORY" STUDENT SET UPS FOR PROBLEM 3; BOTH STUDENTS ARE IN THE EDA SECTION OF THE LABORATORY.

FUTURE WORK

In the Fall 2017 semester, we will implement a fully hybrid laboratory (with 32 students: 16 in each the control and new sections), which would include both manual wiring experience, in addition to advanced EDA tool practice, within each laboratory experiment.

To make sure that students receive adequate training and experience in VHDL, we will use the Codevolve platform (Codevolve.com) to build and deploy interactive hands-on tutorials on VHDL (a sample screenshot of the interface is given below). These exercises are completion-based and will amount to a percentage of the final laboratory grade. Having hands-on, completion-based VHDL tutorials will allow the students to gain sufficient practice with VHDL syntax prior to coming to the laboratory, allowing to off-load some of the pre-laboratory lecture and in-lab troubleshooting to maximize the time spent on designing and analyzing experimental results.



CONCLUSION

In this paper, we have discussed our experience of designing a robust laboratory final examination to evaluate the material and skills retention of students in three different sections of a digital logic design laboratory. The sections were composed primarily of Aerospace and Mechanical Engineering (AE/ME) undergraduate students, where the lecture and lab for this course serve as a service course for several academic majors. Although the results show that students in the hybrid section of the laboratory performed better, as compared with students enrolled in the control section (older-style laboratory sequence), the breadth of knowledge of the students in the hybrid sections (*i.e.,* advanced VHDL concepts, system integration, system design) could not be tested with the assessment tool used, as it was created intending to test baseline knowledge. In addition, an administration fault has skewed the control group results (in an informal survey 29/44 students from the control group have exchanged information about the exam with their peers), so only a limited subset of student data could be used for analysis.

From our previous results [1], it was apparent that the newer approach increases student interest, allows students to realize the relevance of the course toward their major and future career and attain a greater understanding of the presented concepts, when compared to the control group. The results from this study, however, showed that a purely EDA-based approach to digital circuits would put students at a disadvantage when it comes time to creating circuits by hand, troubleshooting, and wiring them.

Overall, the hybrid section of the laboratory fits better with AE/ME disciplines, while providing the same (or better, in some aspects) material retention and engineering thinking. In addition, providing the students balanced exposure to EDA tools and wiring would increase their marketability for defense and commercial aerospace companies.

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